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Modeling the copper microstructure and elastic anisotropy and studying its impact on reliability in nanoscale interconnects

Adarsh Basavalingappa*, Ming Y. Shen and James R. Lloyd

Abstract

Background: Copper is the primary metal used in integrated circuit manufacturing of today. Even though copper is face centered cubic it has significant mechanical anisotropy depending on the crystallographic orientations. Copper metal lines in integrated circuits are polycrystalline and typically have lognormal grain size distribution. The polycrystalline microstructure is known to impact the reliability and must be considered in modeling for better understanding of the failure mechanisms.

Methods: In this work, we used Voronoi tessellation to model the polycrystalline microstructure with lognormal grainsize distribution for the copper metal lines in test structures. Each of the grains is then assigned an orientation with distinct probabilistic texture and corresponding anisotropic elastic constants based on the assigned orientation. The test structure is then subjected to a thermal stress.

Results: A significant variation in hydrostatic stresses at the grain boundaries is observed by subjecting the test structure to thermal stress due to the elastic anisotropy of copper. This introduces new weak points within the metal interconnects leading to failure.

Conclusions: Inclusion of microstructures and corresponding anisotropic properties for copper grains is crucial to conduct a realistic study of stress voiding, hillock formation, delamination, and electromigration phenomena, especially at smaller nodes where the anisotropic effects are significant.

Keywords: Integrated circuit reliability, Thermal stresses, Young's modulus, Microstructure, Stress migration, Electromigration

Background

Research in reliability of interconnects is increasingly important as interconnects are constantly shrinking in dimensions. Stress-induced voiding, hillock formation, and electromigration are some of the prominent reliability concerns for interconnect structures (Suo 2003). Stress induced voiding or stress migration is a failure mechanism that often occurs in interconnects. Voids form as result of vacancy migration driven by the hydrostatic stress gradient. Large voids may lead to open circuit or unacceptable resistance increase that impedes the integrated circuit (IC) performance. High temperature processing of copper dual damascene structures leave the copper with a large tensile stress due to a mismatch in coefficient of thermal expansion (CTE) of the materials involved. The stress can relax with time through the diffusion of vacancies leading to the formation of voids and ultimately open circuit failures (Alers et al. 2005). Electromigration is mass transport due to the momentum exchange between diffusing metal atoms and conducting electrons in the direction of electron flow. If there is a flux divergence, a pressure gradient will be generated opposite to the electromigration induced driving force. If the stress exceeds certain levels, a delamination will occur that leads to a void and eventually an open circuit. The criterion for this delamination is not the hydrostatic stress, but the stress normal to the interface where the delamination is taking place. Thus, with polycrystalline copper, for a given value of the hydrostatic stress, the normal stress at the

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interface where a delamination would take place is a function of the crystallographic orientation of the copper grains in contact with that surface (Lloyd et al. 2006). This results in a bimodal or multi-modal failure distribution where the behavior is a sensitive function of the texture and geometry of the conductor in relation to the flux divergence. Resistance verses time behavior would therefore be very dependent on the location and orientation of a specific grain. The resistance increase can be abrupt, slow, or not measurable depending on the geometry. This has great importance when extrapolating test results with relatively small numbers of samples (dozens at most) to the case of a modern processor that may have hundreds of thousands of potential failure sites (Lloyd et al. 2006).

The stress levels resulting due to mismatch in CTE can also lead to hillock formation, a stress-induced diffusional relaxation process, during the IC fabrication process (Timma et al. 2010; Lin et al. 2001). After depositing capping nitride material at above 380 °C two hillock formation modes were observed: (i) grain boundary sliding mode leading to single grain extrusion hillock and (ii) diffusion dominated hillock formation mode leading to smaller hillocks (Timma et al. 2010). Post nitride hillocks preferentially nucleate at the triple junction of the grain boundary. It is believed that interface Cu/TaN diffusion dominates diffusion mechanism at smaller line dimensions compared to grain boundary diffusion (Timma et al. 2010). The hillocks can be potential area for localized peaks in electric field which can result in early failure by dielectric breakdown. Even though copper has same CTE in all the directions, the anisotropy in elastic moduli of copper leads to development of different stress levels in adjacent grains in turn promoting grain boundary sliding potentially leading to hillock formation.

Primarily, prior works (Oh et al. 2013; Heryanto et al. 2011; Weide-zaage 2012; Wu et al. 2010; O Brien 2013; Hommel et al. 2002; Paik et al. 2004) have considered crystalline copper and isotropic material properties for reliability simulations. A clear dependance between the copper microstructure in nanoscale interconnects, void formation kinetics, and electromigration statistics has been established through experiments (Cao et al. 2013). A significant difference in the electromigration failure lifetime as a function of grain size was observed, large grain structures had 14x higher lifetime compared to small grain structure. The models with single crystal copper overestimates the lifetime and does not provide predictive information related to early fails which play a critical role while extrapolating the lifetimes to use conditions.

In this work we take into account the orientation dependent anisotropic elastic constants of copper to study the evolution of stress levels in the 3 dimensional interconnect structure to better understand the effect of texture and elastic anisotropy of copper on reliability. The presently accepted methods for extrapolation do not take this into consideration. When the extreme extrapolation from about 16 samples to thousands or hundreds of thousands of potential failure sites on a processor chip is made, the predictions would be very pessimistic. But, most importantly, they would be wrong.

Methods

The copper interconnect is known to have microstructure, which is dependent on various factors including copper deposition conditions, thermal processing conditions, seed layer deposition techniques and thickness, seed layer treatment, liner/barrier material types and deposition techniques, and layout geometry (Ceric and Selberherr 2011). Experimental data have shown reliability lifetimes of copper interconnects to be dependent on microstructure, texture distribution, and grain size distribution (KIM 2006; Ryu et al. 1999; Choi et al. 2007; Choi et al. 2008). Further, Copper has a very anisotropic mechanical behavior (Kocks et al. 2000; Yeap et al. 2011) and is known to impact stress voiding and electromigration lifetime (Nucci et al. 1997; Ryu et al. 1997). Hence, it is critical to consider the microstructure and corresponding anisotropy in copper grains while studying reliability of copper interconnects.

Elastic anisotropy of copper

The mechanical behavior of copper is highly anisotropic. Although copper is a face centered cubic crystal like aluminum, the elastic constants of copper vary considerably for different crystallographic orientations. Elastic modulus of Copper is shown in Fig. 1 as a function of direction in 3D space illustrating the anisotropy of Copper. The elastic modulus in [111] direction is 3 times that in [100] direction. This can result in development of stress gradients at the grain boundaries promoting failure.

The relative degree of anisotropy can be expressed by a Zener ratio A (defined as in eq. (1)), where A = 1 for a perfectly isotropic material and A = 3.21 for Cu (obtained by using values C_{11} = 168.4 GPa, C_{12} = 121.4 GPa, and C_{44} = 75.4 GPa (Hertzberg et al. 1983)).

$$A = \frac{2 * C_{44}}{C_{11} - C_{12}} \tag{1}$$

where, C_{11}, C_{12}, and C_{44} are elastic stiffness constants of crystals.

Test structures

Three dimensional simulation test structures were created to represent typical dual-damascene via test structures. Two test structures (a) single crystal copper and

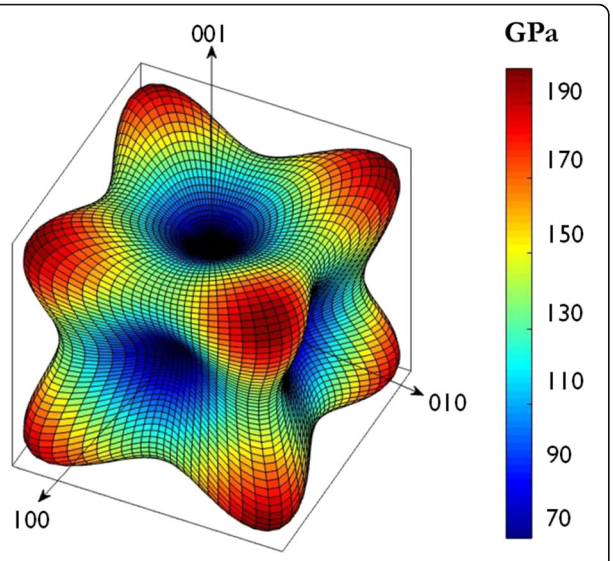

Fig. 1 Elastic moduli of copper as a function of direction

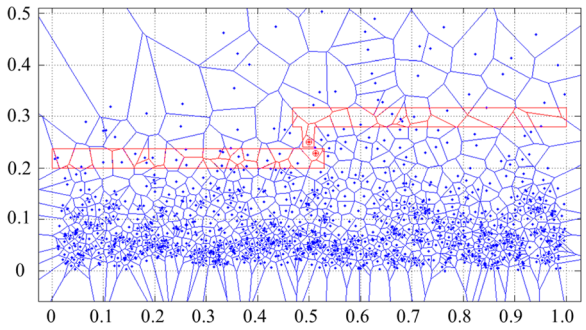

Fig. 2 Original Voronoi Tessellation (*blue*) generated within 1 μm x 1 μm area and (Cu metal) limited Voronoi Tessellation (*red*) forming the polycrystalline metal structure. Dimensions are in microns

(b) polycrystalline copper were created to study the impact of microstructure and Cu anisotropy on the evolution of stress levels with an applied thermal stress.

There is a growing interest in the computation community to use Voronoi tessellation to model microstructures and study their impact (Burtseva et al. 2015; Itakura et al. 2005; Rickman and Barmak 2013; Nabiollahi et al. 2015; Rudd and Belak 2002; Musienko et al. 2007; Piekoś et al. 2008; Gao Guo Jie et al. 2013. A Voronoi diagram in simplest case can be defined as follows: Given a finite set of generating points in a plane, their Voronoi diagram divides the plane into convex polygons containing exactly one generating point, such that, the line segments forming the Voronoi diagram are all the points in the plane that are equidistant to the two nearest generating points.

In order to create polycrystalline metal test structures, a Voronoi tessellation (blue) was generated with MATLAB in a 1 μm x 1 μm area and then limited to the boundary of copper metal line length and height to obtain line limited Voronoi tessellation (red) forming the polycrystalline metal structure (see Fig. 2). The coordinates for each polygon in the limited Voronoi tessellation was extracted from MATLAB and used to define the microstructure of the copper conductors in the test structure generated with the Synopsys TCAD tool (Synopsys 2015) (Fig. 4), Sentaurus Structure Editor. A bamboo polycrystalline structure is observed in metal lines with a lognormal grain size distribution (Cao et al. 2014; Rizzolo 2014; Meyer et al. 2005. A typical observance that grains are smaller at the bottom and larger at the top of the trench as been made from experiments (Cao et al. 2013; Karmarkar et al. 2012; B. Li et al. 2014). In order to obtain lognormal grain size distribution the the points for Voronoi tessellation were generated with random points for x-coordinates (horizontal) and lognormally distributed pseudorandom points for the y-coordinates (vertical). With this approach we obtain smaller grains at the bottom and larger grains at the top as shown in Figs. 2 and 4. The grains with diameter less than 6 nm were merged with adjacent grains to account for smaller grains being consumed by the adjacent larger grains during grain growth. The lognormal probability plot of the grain size distribution obtained by Voronoi tessellation is shown in Fig. 3.

Two 3-dimensional test structure included (a) crystalline Cu metal structure with isotropic elastic constants (Single Crystal), (b) polycrystalline Cu metal structure generated by using lognormal Voronoi tessellation with orientation dependent anisotropic elastic constants to the grains (Large Grains). Cross section of polycrystalline test structure is shown in Fig. 4. The test structures comprised Si substrate, inter level dielectric (ILD) SiCOH, SiCN cap layer, and TaN liner material.

A tapered via structure was implemented in the test structures to replicate a scenario close to real structures. The tapered via was 25 nm at the top and 21 nm at the

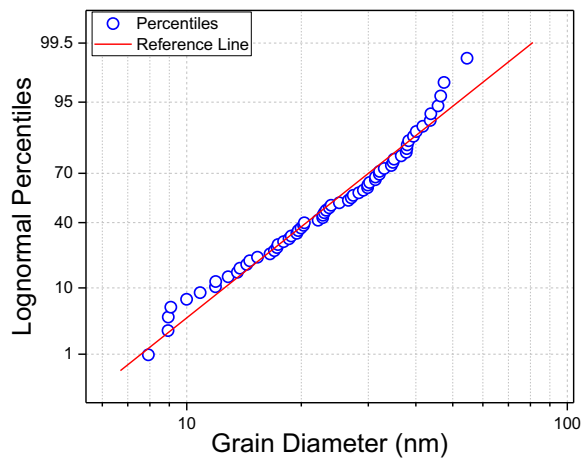

Fig. 3 Log-normal Probability plot of the grain size distribution obtained by Voronoi tessellation after elimination of small grains

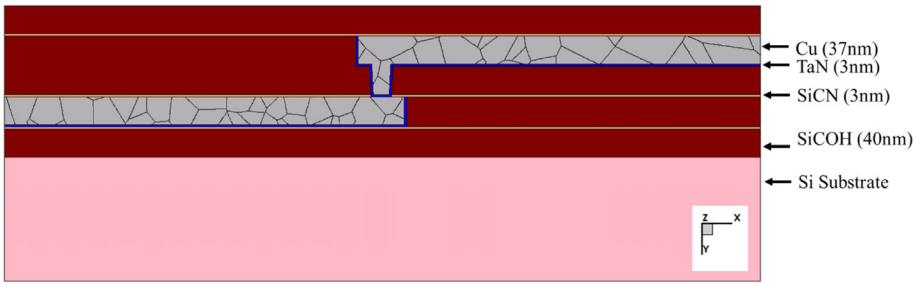

Fig. 4 Cross section of polycrystalline test structure created using Cu metal boundary limited Voronoi tessellation to form the polycrystalline Cu metal structure

bottom. The 3-dimensional test structures were created by encapsulating the copper lines and via with liner/cap material and bounded by SiCOH. This provides better calculation of thermo-mechanical stresses compared to a 2-dimensional simulated test structure which may result in calculated stress levels that may not represent the actual BEOL interconnect structure. The line width of copper used was 22 nm. Average grain size used in the simulation for case b (polycrystal), was ~ 1x line width. Average grain diameter of ~20 nm is observed experimentally for Cu and Cu(Mn) lines for 45, 28, and 22 nm nodes (Cao et al. 2014). Further, electron backscatter diffraction (EBSD) top-view studies of 60 nm wide copper lines have shown nearly no grain boundaries parallel to the trenches, indicating a polycrystalline bamboo structure (Meyer et al. 2005. Hence, it is a simplistic yet reasonable assumption that a single grain extends along the width of the line for the 22 nm line widths used in this work.

Grain oreintation assignment

Numerous studies have shown copper interconnects to be textured (Muppidi et al. 2005; Ganesh et al. 2010; Kaouache et al. 2008; Rizzolo 2014), i.e. to have preferred orientation. The preferential orientation of copper grains is observed to be dependent on the line scaling and process conditions (Zhang et al. 2009; Ganesh et al. 2012; Chen 2015). Prior work (Rizzolo 2014) has observed texture in 70 nm patterned copper lines with 35% of the grains having (111) orientations, 21% (100) orientations, and 14% (110) orientations along the trench normal. The remaining 30% grains had other orientations. Whereas, (Cao et al. 2013; Cao et al. 2014) have observed a preferred orientation of (110) along the trench normal and (111) along the trench width in 70 nm patterned copper lines. This difference in preferred orientation could possibly be due to different processing conditions.

In this work, statistical information from (Rizzolo 2014) was used, and each grain in the microstructure corresponding to test structure (b) was randomly assigned one of (111), (100), (110), (311), (511), (221), (321), (310), (210), (211), (331), (7 5 13), and (11 1 11) orientations with a probability of 35, 21, 14, 3, 3, 3, 3, 3, 3, 3, 3, 3, and 3% respectively. These grains were assigned corresponding elastic constants of Cu based on the assigned orientation. The anisotropic material properties for the copper are defined along three planes of symmetry that are parallel to the crystal axes. In the simulation coordinate system, the axes are aligned along the three planes of symmetry. The material properties are defined using Young's moduli in the symmetry planes (E_1, E_2, and E_3) (see Table 1). The CTE and Poisson ratio of copper were kept constant for all the cases at 17.7 μm/m/K and 0.28 respectively. The grain orientation and corresponding material properties assignment was conducted using Sentaurus Interconnect tool.

Thermal stress

Deposition of copper, liner, and ILD is typically performed at high temperatures. Since the CTE of copper is high compared to other materials involved, when the

Table 1 Young's modulus of Copper

Material	Young's modulus [GPa]		
	E_1	E_2	E_3
Isotropic	120	120	120
Orientation 1 (100)	66.7	66.7	66.7
Orientation 2 (110)	66.7	130.3	130.3
Orientation 3 (111)	130.3	191.1	130.3
Orientation 4 (311)	130.3	96.2	130.3
Orientation 5 (511)	130.3	77.2	130.3
Orientation 6 (221)	158.3	158.3	158.3
Orientation 7 (321)	130.3	130.3	191.1
Orientation 8 (310)	130.3	80.9	130.3
Orientation 9 (210)	158.3	97.0	158.3
Orientation 10 (211)	130.3	130.3	130.3
Orientation 11 (331)	130.3	143.6	130.3
Orientation 12 (7 5 13)	66.7	122.2	191.1
Orientation 13 (11 1 11)	130.3	131.3	130.3

interconnect structure along with the substrate is cooled down from the elevated temperatures to room temperature, copper would want to shrink more than the other materials. This leads to formation of thermally induced stress σ_{th}, as in

$$\sigma_{th} = E\Delta\alpha\Delta T \quad (2)$$

where, E is appropriate elastic modulus, Δα is relative coefficient of thermal expansion of the material, and ΔT is the difference in temperature, i.e., difference between deposition or stress free temperature and observation temperature in this case. Due to high CTE of copper, the stresses generated within copper are tensile when the structure is at temperature lower than the deposition temperature (Vinci et al. 1994; Marcus et al. 1994).

In cases where the initial stress due to thermal processing or the cumulative stress from the fabrication process and the thermal stress at elevated observation temperature reaches a critical value, it may result in stress induced voiding. Whereas in other cases where the initial stress is not sufficient enough to cause stress induced voiding, in the presence of current flow, the residual thermal stress and the electromigration-induced stress add up. Depending on the initial stress profile within the interconnect structure and the current flow direction, the threshold required to nucleate void can be rapidly reached under undesired conditions. Once the void is formed, the normal stresses at the void surface vanishes leaving behind a high stress gradient in the same direction as electromigration, which will drive the void growth (Lloyd 1999).

Since accelerated tests to obtain reliability lifetimes are typically performed at elevated temperatures, we simulate similar phenomenon to study the impact on evolution of stress levels within the test structures. The Cu interconnect structures were assumed to be cooled from the stress free temperature 400 °C to the testing temperature or use condition of 100 °C, similar to (Rhee et al. 2003). This basically gives a delta of -300 °C, which accounts for deposition/recrystallization-anneal conditions of copper interconnect and the test condition. Grain growth and recrystallization at elevated temperatures were however not taken into consideration in this work. Assuming the grains are fixed, simulations were conducted to study the impact of thermal stress using Sentaurus Interconnect tool.

Results and discussion

The process conditions, materials used, processing temperatures etc., cause tensile or compressive stress in the interconnect structure. Numerous prior experimental observations have shown that failure possibility is increased with tensile stress at the interfaces (Lloyd and Clement 1995).

As a result of the thermal stress, i.e., cooling from the stress free temperature 400 °C to the testing temperature 100 °C, a significant difference in normal stresses (Fig. 5) were observed for the crystalline test structure without Cu grains by using isotropic elastic constants of Cu (Fig. 5a) which we know is unrealistic, but is commonly assumed and test structures with polycrystalline Voronoi tessellation based microstructures (Fig. 5b) of Cu using anisotropy in the elastic constants of Cu. Fig. 5b shows the normal component of the node stresses for the Voronoi based test structures resulting in peak stress values at the grain boundaries based on crystallographic orientation and location of the Cu grains along the Y direction. Note that Fig. 5 is a tilted view of 3-dimenional test structures showing stress levels only in copper while hiding other materials.

Cross section view of the test structures in the middle of copper line width is shown in Fig. 6. High concentration of tensile stress (positive normal stress value) in copper is observed in the via. However, it must be noted that the actual stress values are very dependant on the orientation of the grains in the copper. Fig. 7 shows normal stress in Y direction along a cut-line (shown in inset figure) close to the top of the bottom M1 metal line for

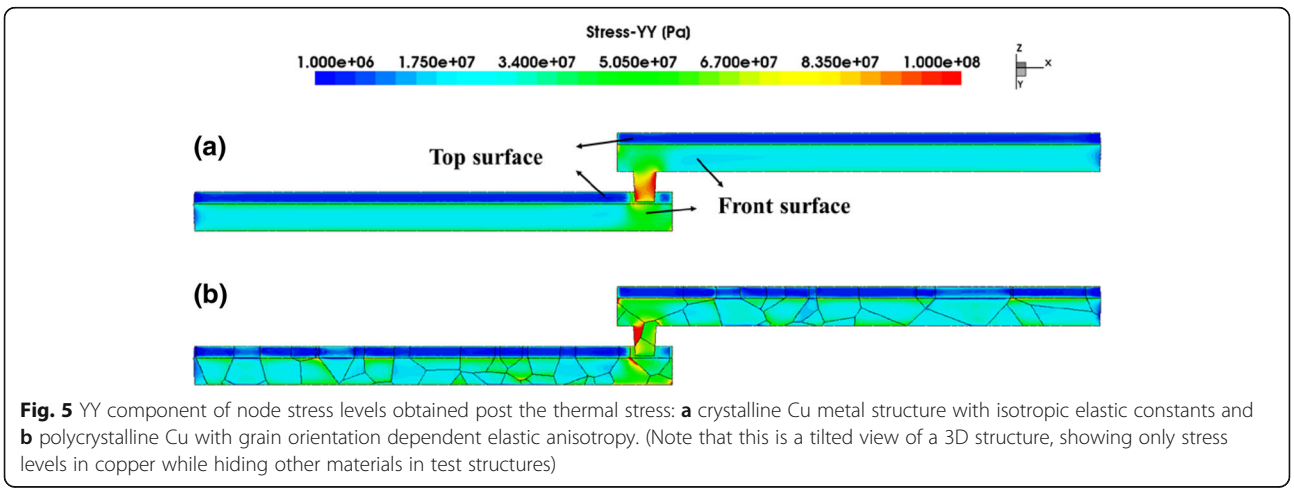

Fig. 5 YY component of node stress levels obtained post the thermal stress: **a** crystalline Cu metal structure with isotropic elastic constants and **b** polycrystalline Cu with grain orientation dependent elastic anisotropy. (Note that this is a tilted view of a 3D structure, showing only stress levels in copper while hiding other materials in test structures)

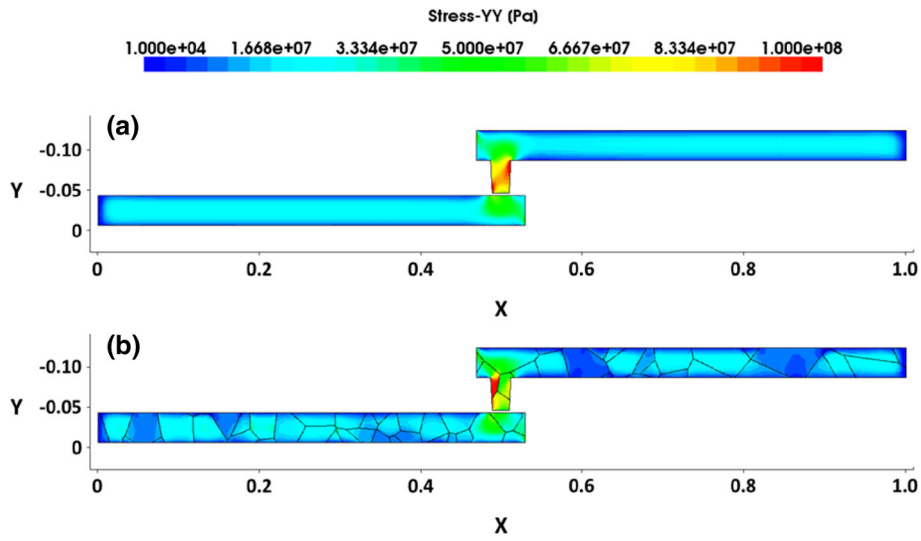

Fig. 6 Cross section of test structure in Fig. 5 showing YY component of node stress levels obtained post the thermal stress: **a** crystalline Cu metal structure with isotropic elastic constants and **b** polycrystalline Cu with grain orientation dependent elastic anisotropy

the two test structures (a) single crystal and (b) polycrystal Cu line. We observe a clear difference in normal stress between crystalline and polycrystalline copper. Polycrystalline copper can result in higher or lower stress levels compared to single crystal structure depending on the microstructure and the grain orientation. Stress induced voiding is typically observed at the bottom of the via. In the presence of no grains towards the bottom of the via, two peaks in normal stresses are observed towards the edge of the via.

During the fabrication process there is more freedom for stress relaxation in the Y direction as the ICs are built layer by layer in the Y direction. Depending on processing conditions and orientation of the grains, some of the grains may have higher stress levels compared to the others thereby leading to hillock formation as observed in (Timma et al. 2010; Lin et al. 2001).

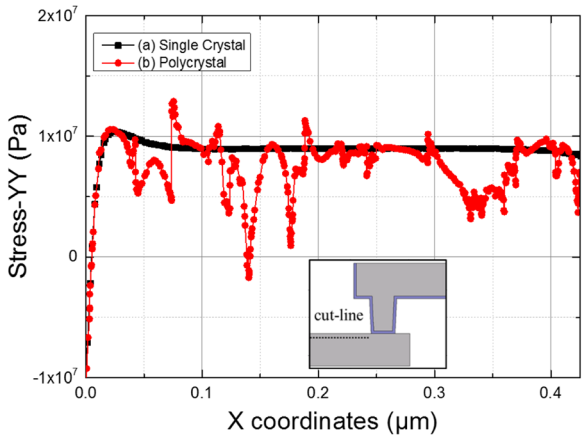

Fig. 7 Normal Stress plot of Cu metal lines along a cut line in M1 close to the top (cutline shown in inset figure): **a** crystalline Cu metal structure with isotropic elastic constants and **b** polycrystalline Cu with grain orientation dependent elastic anisotropy

Depending on the grain boundary distribution, the polycrystalline structure can result either in a more reliable structure or a less reliable structure compared to a single crystal structure when only normal stress based delamination is considered. However, when we consider stress migration which is primarily driven by the hydrostatic stress gradient which typically have local maxima at the grain boundaries the polycrystalline structures might result in easier nucleation of voids along grain boundaries and also growth of voids (Yang et al. 2011; Zschech et al. 2009; Sukharev et al. 2009). Stress migration and electromigration induced mass transport along the copper interconnects is dependent on competing activation energies for atomic migration along Cu/SiCN interface, Cu/TaN interface, and copper grain boundaries (Hau-Riege and Thompson 2001; Ogawa et al. 2002; Sukharev and Zschech 2004).

Pressure (negative hydrostatic stress) levels were observed for the two test structures Fig. 8a crystalline test structure, without Cu grains by using isotropic elastic constants of Cu from Table 1 and Fig. 8b with polycrystalline Voronoi tessellation based microstructures of Cu using anisotropy in the elastic constants of Cu and textured grain orientation. Pressure, is one-third of the negative of the trace of the stress tensor

$$P = -\frac{1}{3}\sum_i \sigma_{ii} = -\sigma_H \tag{3}$$

where, P is pressure, σ_{ii} is stress tensor, and σ_H is hydrostatic stress.

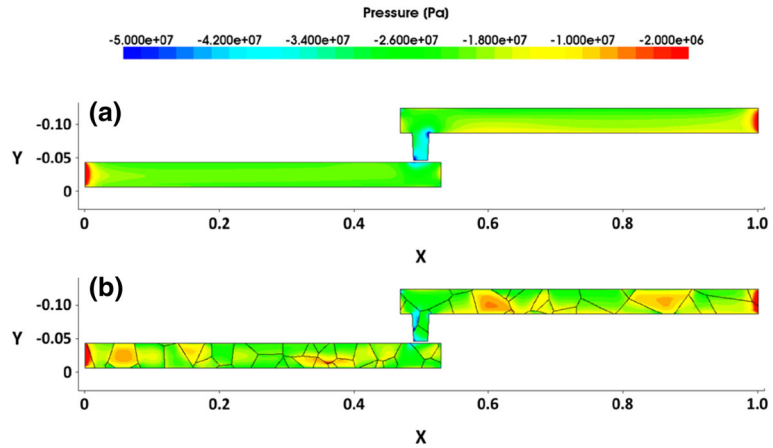

Fig. 8 Cross section of test structures showing pressure levels obtained post the thermal stress: **a** crystalline Cu metal structure with isotropic elastic constants and **b** polycrystalline Cu with grain orientation dependent elastic anisotropy

A clear variation in the pressure values with the grains in polycrystalline structures is observed unlike the single crystal test structure. Further, higher values of tensile hydrostatic stress are observed with polycrystalline test structure compared to the crystalline case.

Reduction in the overall free energy is typically the driving force for grain growth. The presence of grain to grain variation in pressure values (or variation in strain energies) may act as a driving force to promote grain growth (Thompson 2000; Wang et al. 2013; Gianola et al. 2006; J. C. M. Li 2006; Zhang et al. 2005; Zielinski et al. 1995).

Pressure values in the middle of Cu line width are plotted in Fig. 9 along a cutline through center of bottom metal line, center of liner, center of via, and center of top metal line as shown in the inset of Fig. 9. A significant variation in pressure values were observed by

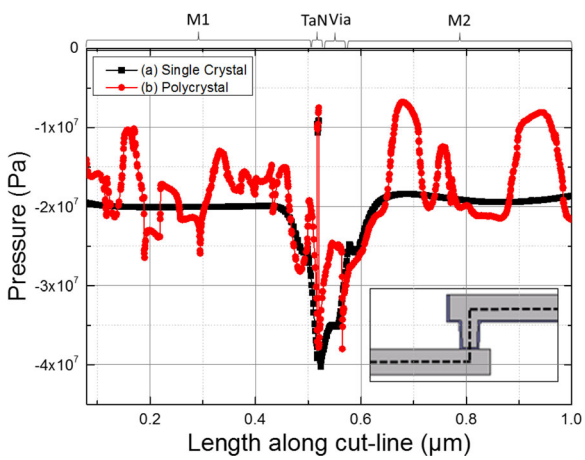

Fig. 9 Pressure plot of Cu metal lines along M1/Ta-liner/Via/M2 (cutline shown in inset figure): **a** crystalline Cu metal structure with isotropic elastic constants and **b** polycrystalline Cu with grain orientation dependent elastic anisotropy

including polycrystalline test structures compared to the crystalline structure. The gradient of the hydrostatic stress acts as a driving force for mass transport. There will be a chemical potential to make the stress uniform through diffusion. In case of flux divergence, a hydrostatic stress gradient will be generated opposite to the electromigration induced driving force. We observe extreme pressure gradient values being concentrated at the grain boundaries. This is more clearly evident from Fig. 9 where we observe changes in the pressure values at the grain boundaries leading to high pressure gradient values unlike the single crystal case. It is this pressure gradient which plays a crucial role in mass transport of the copper atoms which will in turn lead to voids and failure of interconnects. The elastic anisotropy in the grains will give rise to high pressure gradients at the grain boundaries. The variation in the stress levels increased with the number of grains indicating that smaller grains are likely to lead to more potential failure sites and might make it easier to reach the critical value required to initiate failure, and in turn lead to less reliable interconnects. Fig. 8 shows high pressure gradient values being concentrated near via and at the grain boundaries making them the potential sites for early fails.

It is only by including polycrystalline structure and corresponding anisotropic properties we can explain the failure modes which are commonly observed, where the failure happens away from the via at a certain grain boundary location within the metal line as in Ref. (Sukharev et al. 2009; Fischer et al. 2001; Baklanov et al. 2012. If we only consider the single crystal test structure the failure happens at the same location at a fixed lifetime for a given stress condition. However, in reality there will be a spread in failure lifetimes for integrated circuit chips even from the same wafer and bimodal and multimodal failure is commonly observed (Ogawa et al.

2002; Fischer et al. 2000; Fischer et al. 2001; Baklanov et al. 2012). This can be explained by considering the randomness involved in the grain distribution. A realistic and predictable simulation of reliability lifetime should include statistical simulations involving the distribution of polycrystalline test structures. Hence, it is of immense importance to consider the polycrystalline test structure and corresponding anisotropic properties for conducting predictable studies of reliability lifetimes of interconnect structures.

Conclusions

In conclusion, Voronoi tessellation based copper microstructure with lognormal distribution of grain sizes was created and used in test structure with textured assignment of orientation and corresponding anisotropic elastic constants to each grain in the microstructure. By subjecting the test structure to a thermal stress, a significant variation in normal stresses and pressure were observed at the grain boundaries. This variation in normal stresses and pressure at the grain boundaries is dependent on the orientation, dimensions, surroundings, and location of the grains. This may introduce new weak points within the metal line where normal stresses can be very high depending on the orientation of the grains leading to delamination and accumulation site for vacancies. Inclusion of microstructures with lognormal grain size distribution and corresponding anisotropic properties for copper grains is critical to conducting a realistic study of the thermal stress induced failure phenomenon especially at smaller nodes where the anisotropic effects are significant.

Abbreviations

CTE: Coefficient of Thermal Expansion; EBSD: Electron backscatter diffraction; IC: Integrated Circuit; TCAD: Technology computer aided design

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Availability of data and materials

Research data for this paper is available upon request from the corresponding author.

Authors' contributions

AB and JRL conceived the work; AB and MYS conducted brainstorming and debugging of the modeling work; AB developed and carried out the modeling work; JRL supervised the work. All authors contributed to the writing and editing of the paper. All authors read and approved the final manuscript.

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Competing interests

The authors declare that they have no competing interests.

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